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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,421	06/30/2003	Volkan Kursun	000687-00302	8087

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/608,421	KURSUN ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-9 and 16-49* is/are pending in the application.

4a) Of the above claim(s) *19-25,27-33,35-41 and 43-49* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-9, 16-18, 26, 34, 42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 26, 34, and 42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation recites "operational phase" is indefinite and vague because operation phase can be anything that regard to the circuit (e.g. input signals phase, performance circuit phase, noise immunity phase, etc.). Clarification is required.

3. claim 9 is rejected as dependent on claim 34.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 2- are rejected under 35 U.S.C. 102(e) as being anticipated by Krishnamurthy et al (6,346,831).

Claim 2, Krishnamurthy shows a domino logic circuit (Figs. 6, 7, 8), comprising;

a pulldown circuit (M19, Fig. 6 or M21-0 to M22-X, Fig. 7) having a dynamic node (A, Fig. 6, or Q, Figs. 7-8);

a keeper (M16, M24 or M33) connected to the pulldown circuit at the dynamic nodes and

a source (174, Fig. 6) of a body bias voltage, the source of the body bias voltage being connected to the keeper to supply the body bias voltage to the keeper to bias the keeper wherein the body bias voltage is a reverse body bias voltage (col. 7, lines 45-48).

Claim 3, Krishnamurthy shows the domino logic circuit of claim 2, wherein the reverse body bias voltage is static (constant voltage, col. 7, lines 48-50).

Claim 4, Krishnamurthy shows the domino logic circuit of claim 3, further comprising a foot transistor (M20, Fig. 6) for connecting the pulldown circuit to ground (Vss).

Claim 5, Krishnamurthy shows the domino logic circuit of claim 3, wherein the pulldown circuit (MN1-0 to M22-X, Fig. 7) is connected to ground without an intervening foot transistor.

Claim 6, Krishnamurthy shows the domino logic circuit of claim 2, wherein the source supplies the reverse body bias voltage such that the reverse body bias voltage alternates between two values (changing voltages, col. 7, lines 48-50).

Claim 7, Krishnamurthy shows the domino logic circuit of claim 6, further comprising a foot transistor (M20, Fig. 6) for connecting the pulldown circuit to ground.

Claim 8, Krishnamurthy shows the domino logic circuit of claim 6, wherein the pulldown circuit (MN1-0 to M22-X, Fig. 7) is connected to ground without an intervening foot transistor.

Claim 16, Krishnamurthy shows a domino logic circuit (Figs. 6-8), comprising:

a pulldown circuit (M19, Fig. 6 or M21-0 to M22-X, Fig. 7) having a dynamic node (A, Fig. 6 or Q, Figs 7-8);

a keeper (M16 or M24) connected to the pulldown circuit at the dynamic node; and

a source of a body bias voltage (174, Fig. 6), the source of the body bias voltage being connected to the keeper (Vbbn) to supply the body bias voltage to the keeper to bias-the keeper;

wherein source supplies the body bias voltage such that the body bias voltage alternates (changing voltages, col. 7, lines 48-50) between a first forward body bias voltage value (col. 7, lines 19-22) and a second reverse body bias voltage value (col. 7, lines 45-48).

Claim 17, Krishnamurthy shows the domino logic circuit of claim 66, further comprising a foot transistor (M20, Fig. 6) for connecting the pulldown circuit to ground.

Claim 18, Krishnamurthy shows the domino logic circuit of claim 16, wherein the pulldown circuit (MN1-0 to M22-X, Fig. 7) is connected to ground without an intervening foot transistor.

Claim 26, Krishnamurthy shows the domino logic circuit of claim 6, wherein the source supplies the reverse body bias voltage such that the reverse body bias voltage

alternates between the two values in accordance with an operational phase (mode is consider as operational phase since the changing voltages are apply between performance and noise immunity, col. 7, lines 49-50) of the domino logic circuit.

Claim 42, Krishnamurthy shows the domino logic circuit of claim 16, wherein the source supplies the body bias voltage such that the body bias voltage alternates between the forward body bias voltage (performance) and the second reverse body bias voltage (noise immunity) in accordance with an operational phase of the domino logic circuit (mode is consider as operational phase since the changing voltages are apply between performance and noise immunity, col. 7, lines 49-50).

Claim 34, Krishnamurthy shows the a domino logic circuit (Figs. 6-8), comprising:

a pulldown circuit (M21-0 to M22-X, Fig. 7) having a dynamic node (Q);

a keeper (M24) connected to the pulldown circuit at the dynamic node; and

a source (174, Fig. 6) of a body bias voltage, the source of the body bias voltage (Vbbn) being connected to the keeper to supply the body bias voltage to the keeper to bias the keeper;

wherein the source supplies the body bias voltage such that the body bias voltage alternates between two values (changing voltages, col. 7, lines 49-50); and

wherein the source supplies the body bias voltage such that the body bias voltage alternates between the two values in accordance with an operational phase of the domino logic circuit (changing voltage s depending on the mode of the circuits, col. 49-50).

Claim 34, Krishnamurthy shows the domino logic circuit of claim 34, wherein the body bias voltage is a forward body bias voltage (col. 7, lines 19-22).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Krishnamurthy et al. (6,204,696) discloses a domino circuit with a keeper having body bias voltages apply to it.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-F (8:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

12/15/05

ANH Q. TRAN
PRIMARY EXAMINER